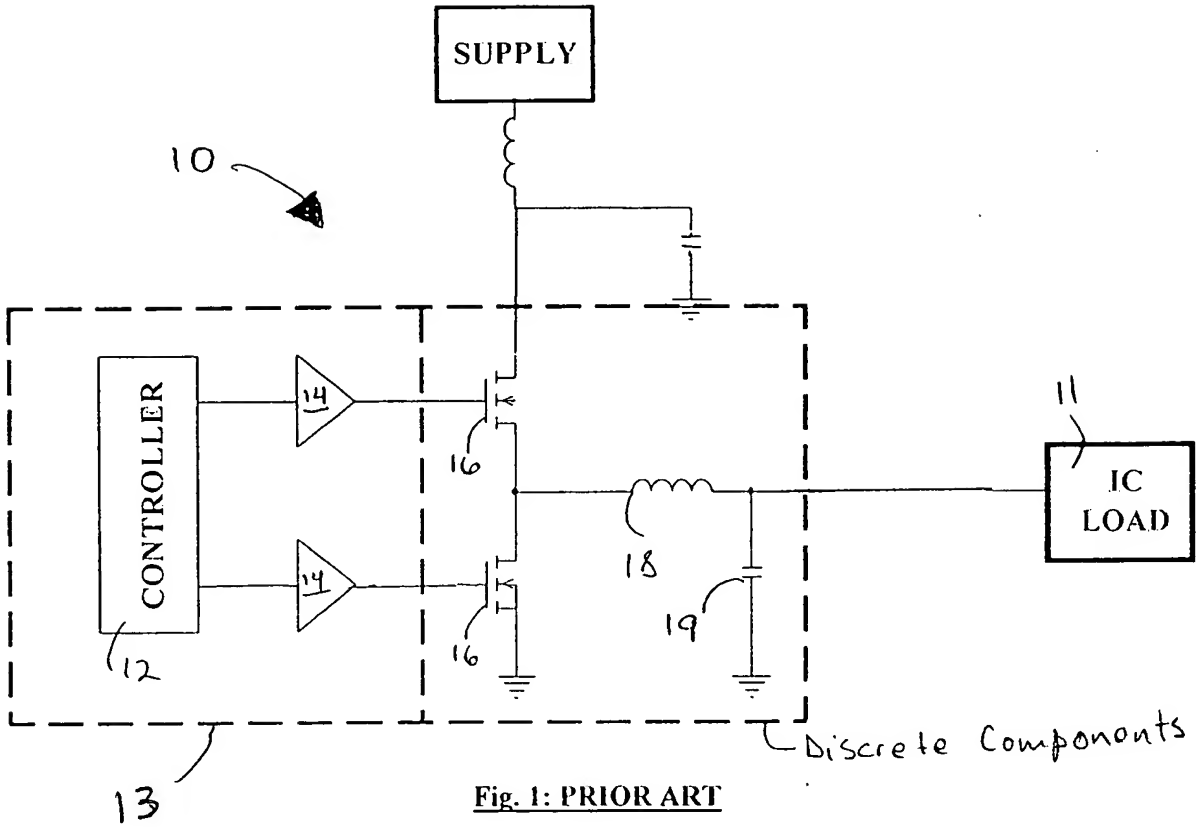

Fig. 1: PRIOR ART

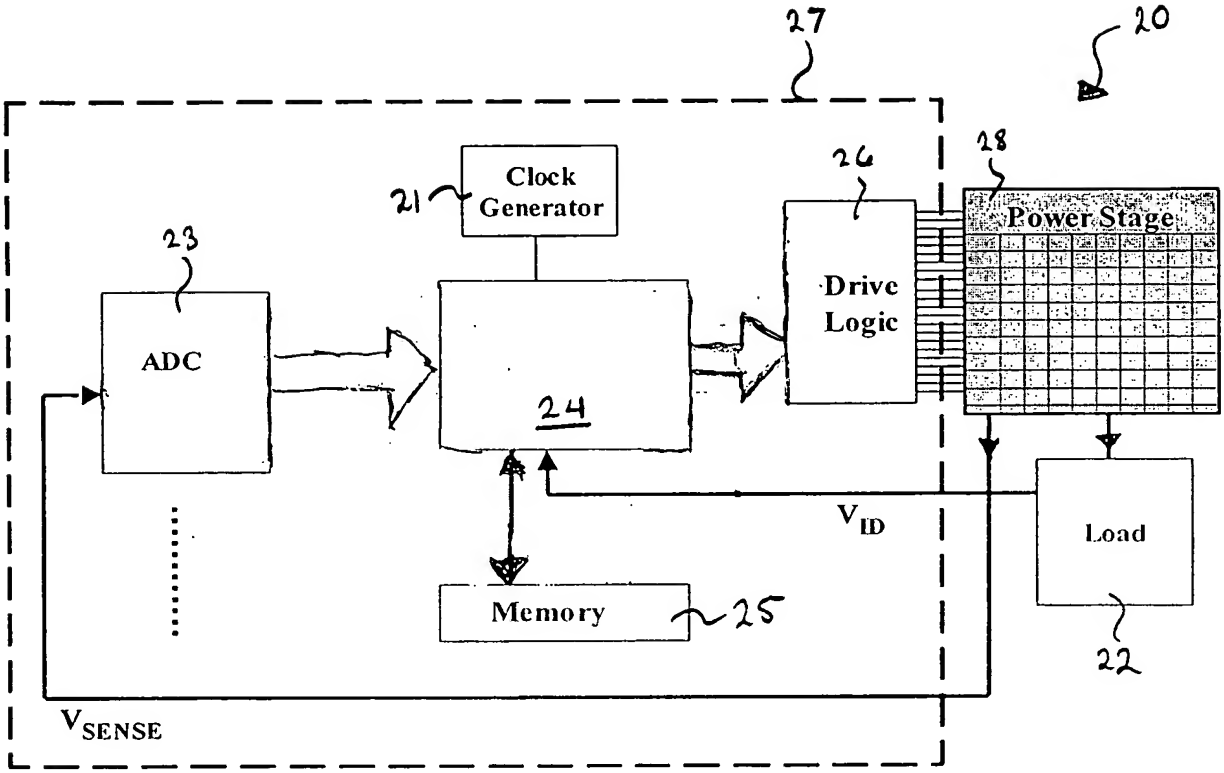
27
20
Clock Generator
21
26
28
Power Stage
23
ADC
Drive Logic
24
V_{ID}
Load
22
Memory
25
V_{SENSE}

Fig. 2

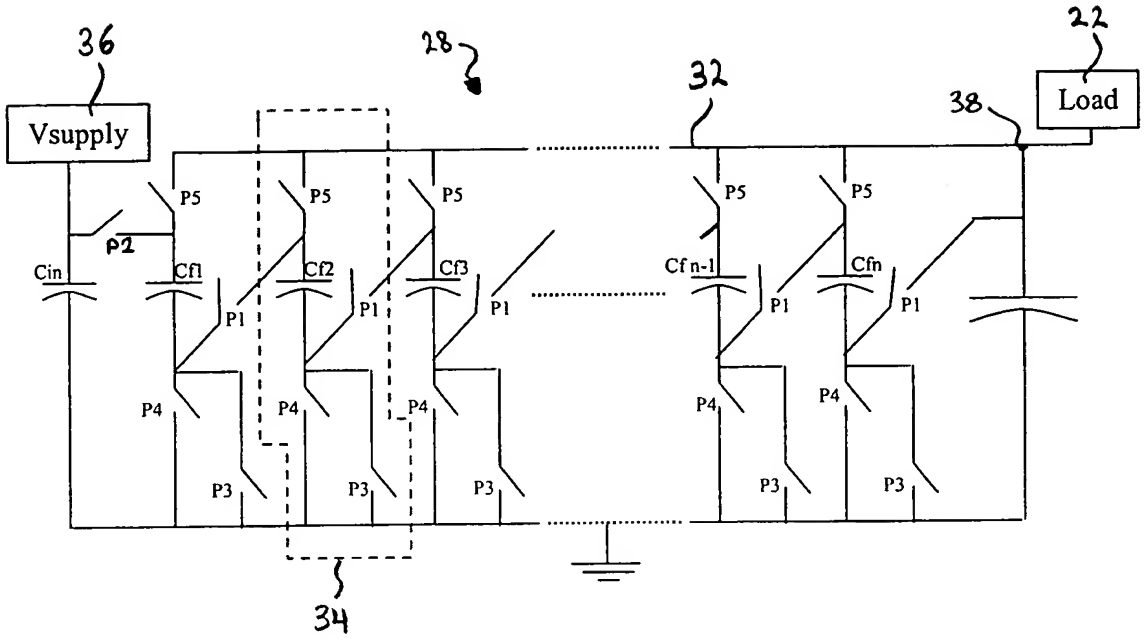
36
28
32
22
38
Load
Vsupply
P5
P2
Cin
Cf1
Cf2
Cf3
Cf n-1
Cfn
P1
P4
P3
34

Fig. 3

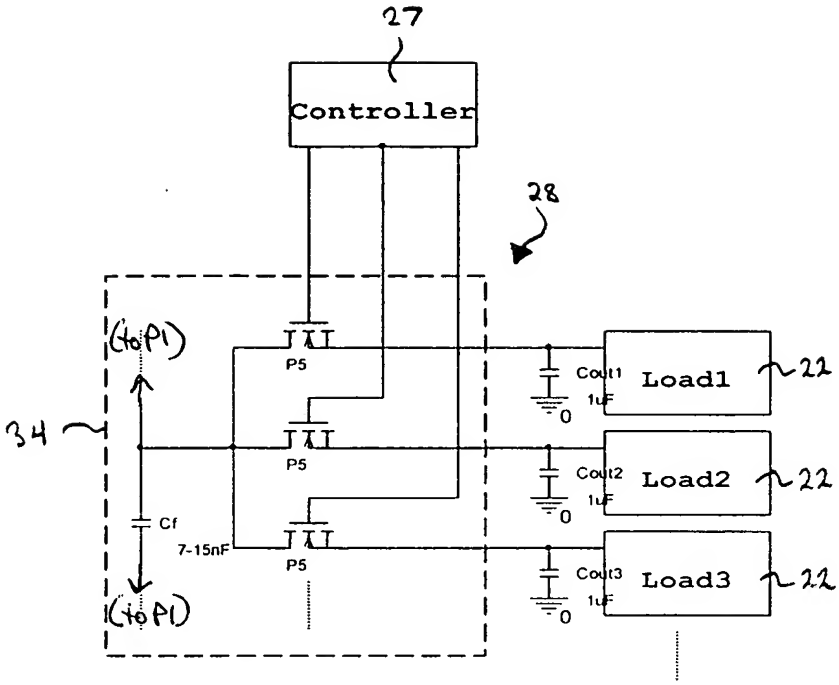
27
Controller
28
(to P1)
34
P5
P5
P5
Cf
7-15nF
(to P1)
Cout1
1uF
Load1
22
Cout2
1uF
Load2
22
Cout3
1uF
Load3
22

Fig. 4

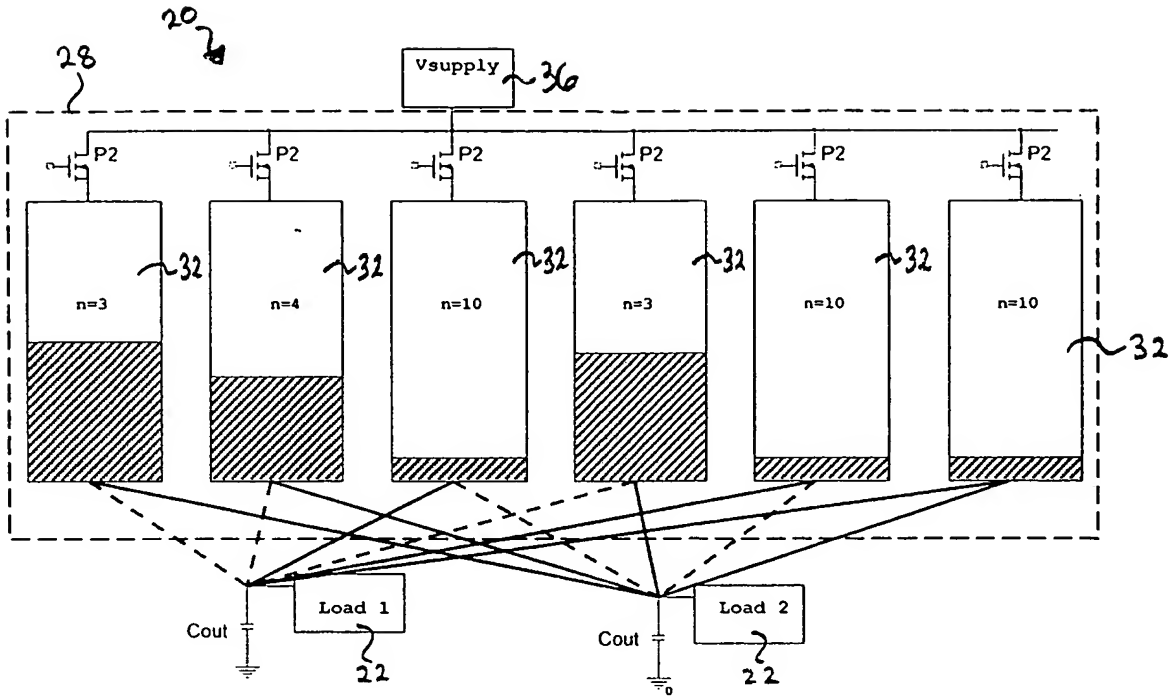
20
28
Vsupply
36
P2
P2
P2
P2
P2
P2
32
32
32
32
32
32
n=3
n=4
n=10
n=3
n=10
n=10
Cout
Load 1
22
Cout
Load 2
22

Fig. 5

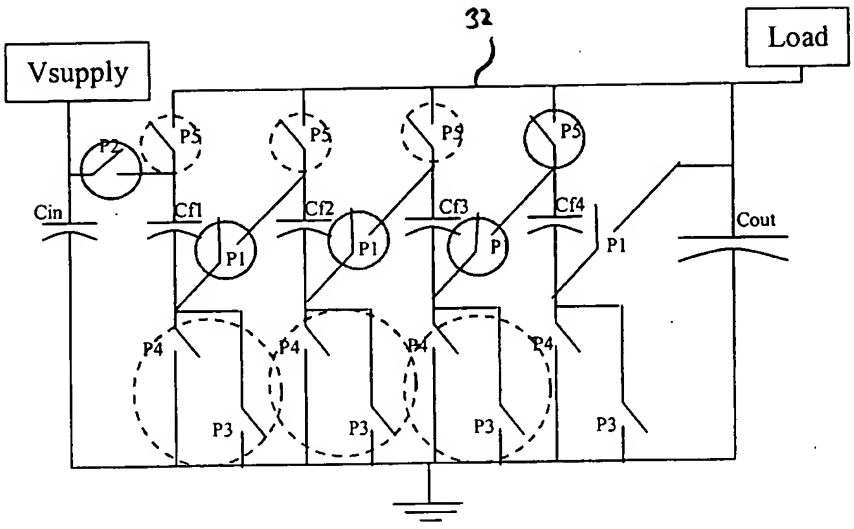
32
Load
Vsupply
P2
P5
P3
P3
P5
Cin
Cf1
Cf2
Cf3
Cf4
Cout
P1
P1
P1
P1
P4
P4
P4
P4
P3
P3
P3
P3

Fig. 6

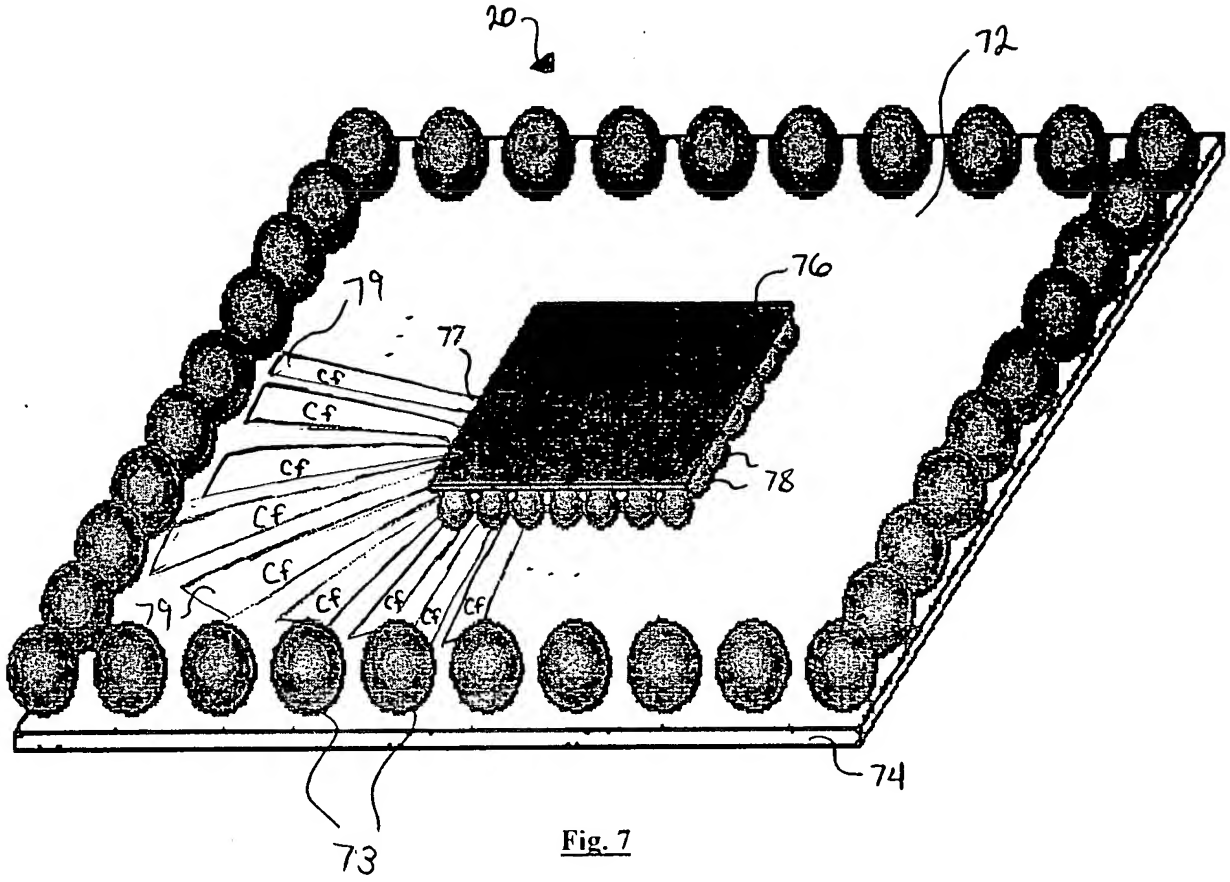

Fig. 7

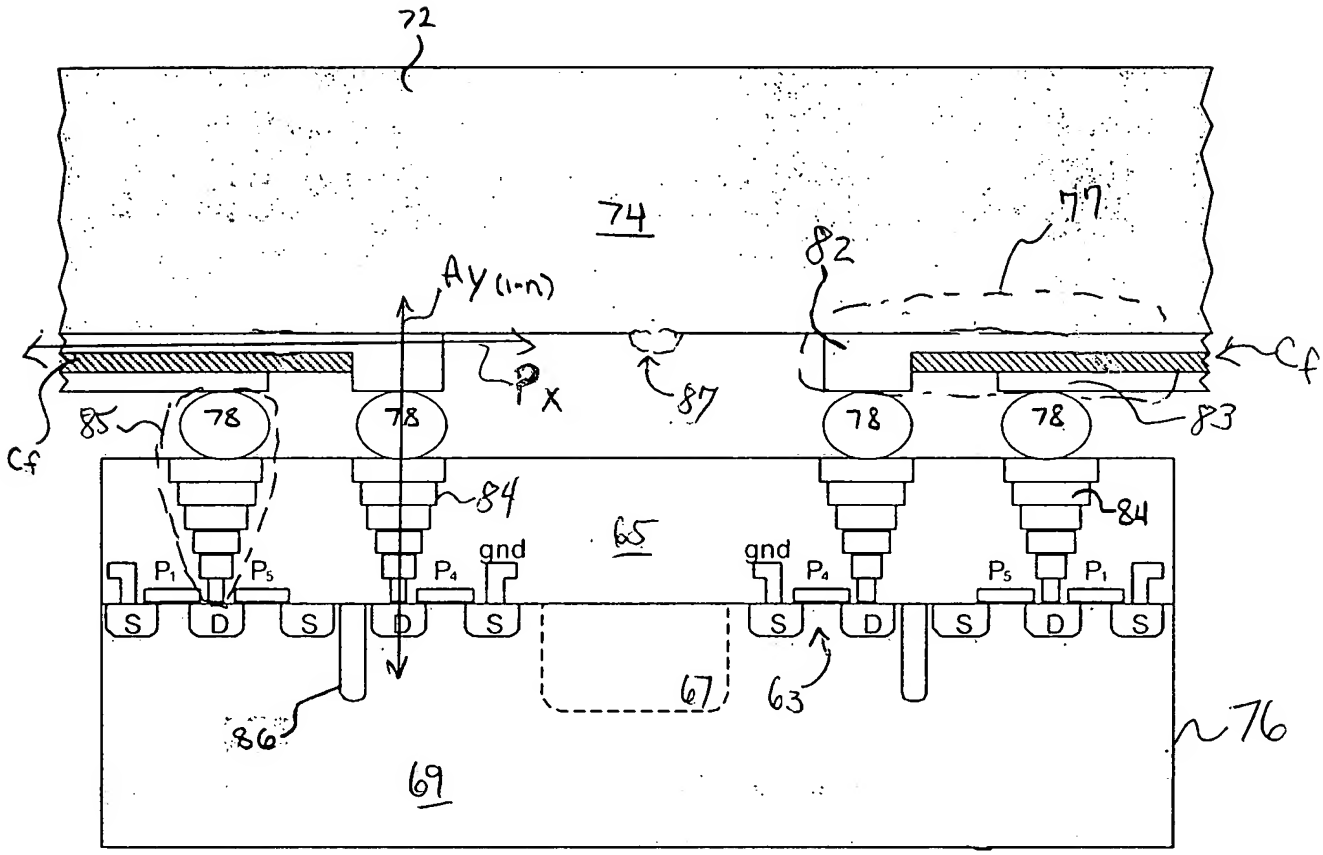
72
74
77
82
Ay (1-n)
Px
87
Cf
Cf
85
78
78
78
78
83
84
84
65
gnd
gnd
P1
P5
P4
P4
P5
P1
S
D
S
D
S
S
D
S
D
S
67
63
86
76
69

Fig. 8

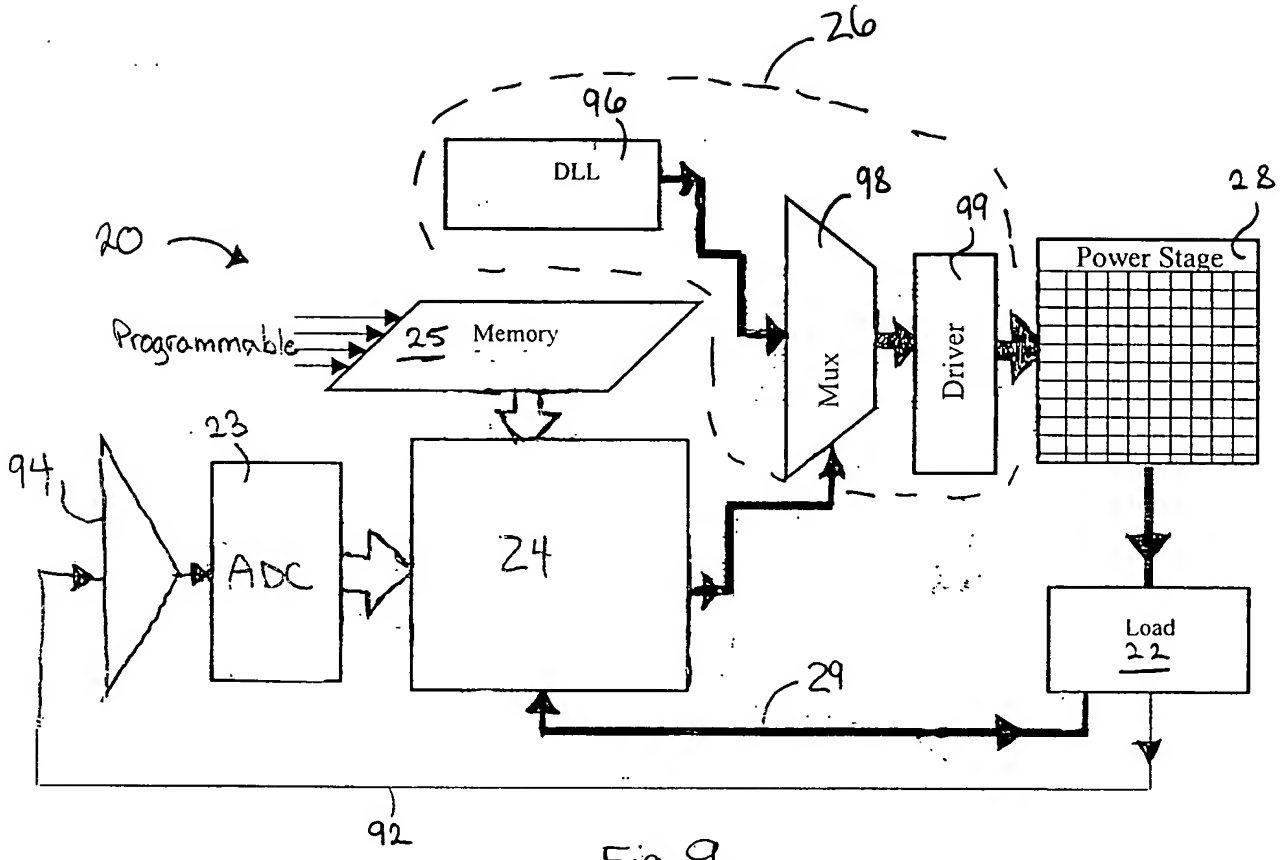
26
96
DLL
98
99
28
20
Power Stage
Programmable
25 Memory
Mux
Driver
23
94
ADC
24
Load
22
29
92

Fig. 9

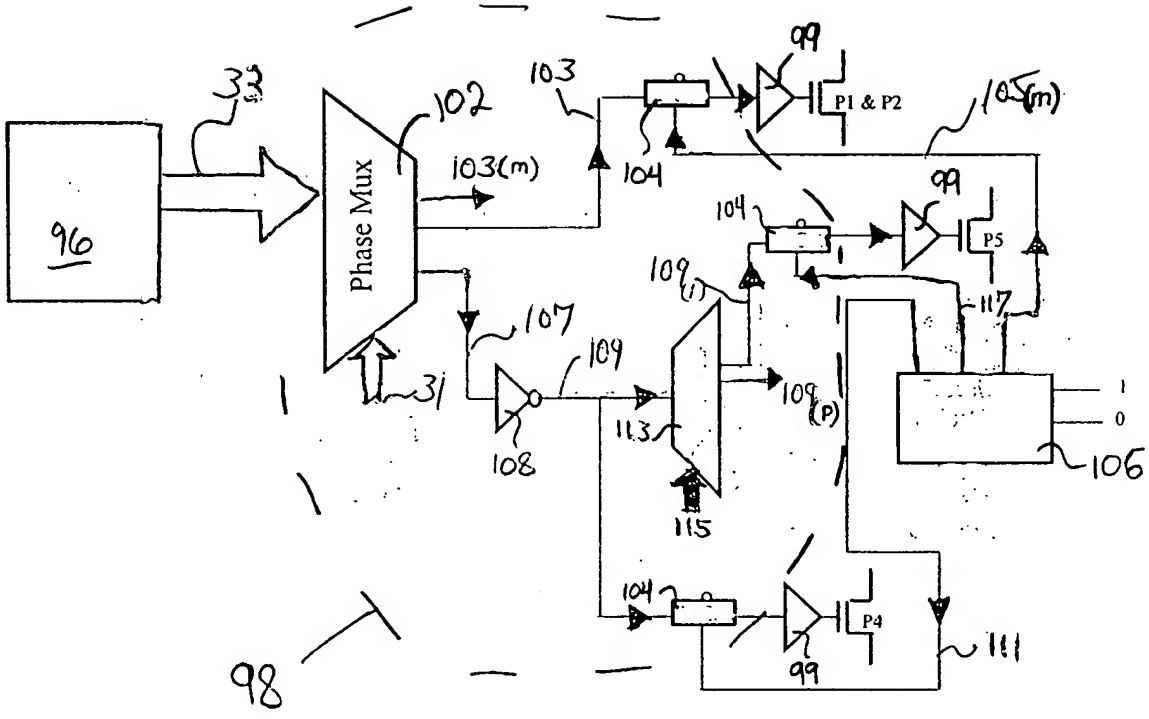
96
33
Phase Mux
102
103
103(m)
104
99
P1 & P2
105(m)
104
99
P5
117
109(1)
107
109
31
108
113
109(P)
115
106
1
0
104
P4
99
111
98

Fig. 10

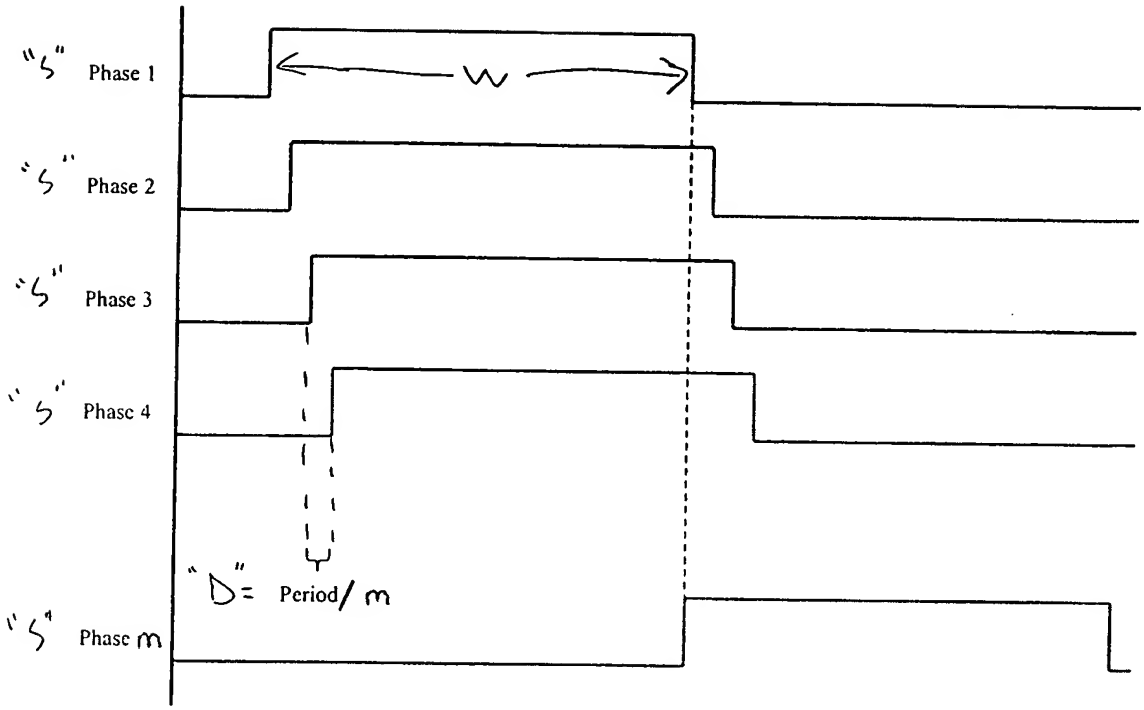

Fig. 11

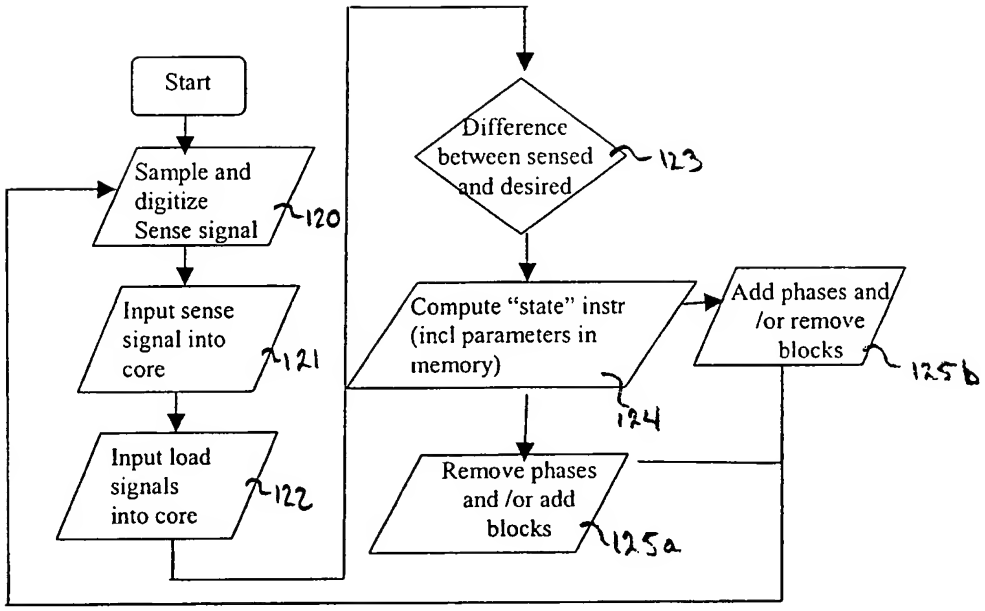
Start
Sample and digitize Sense signal
120
Input sense signal into core
121
Input load signals into core
122
Difference between sensed and desired
123
Compute "state" instr (incl parameters in memory)
124
Add phases and /or remove blocks
125b
Remove phases and /or add blocks
125a

Fig. 12

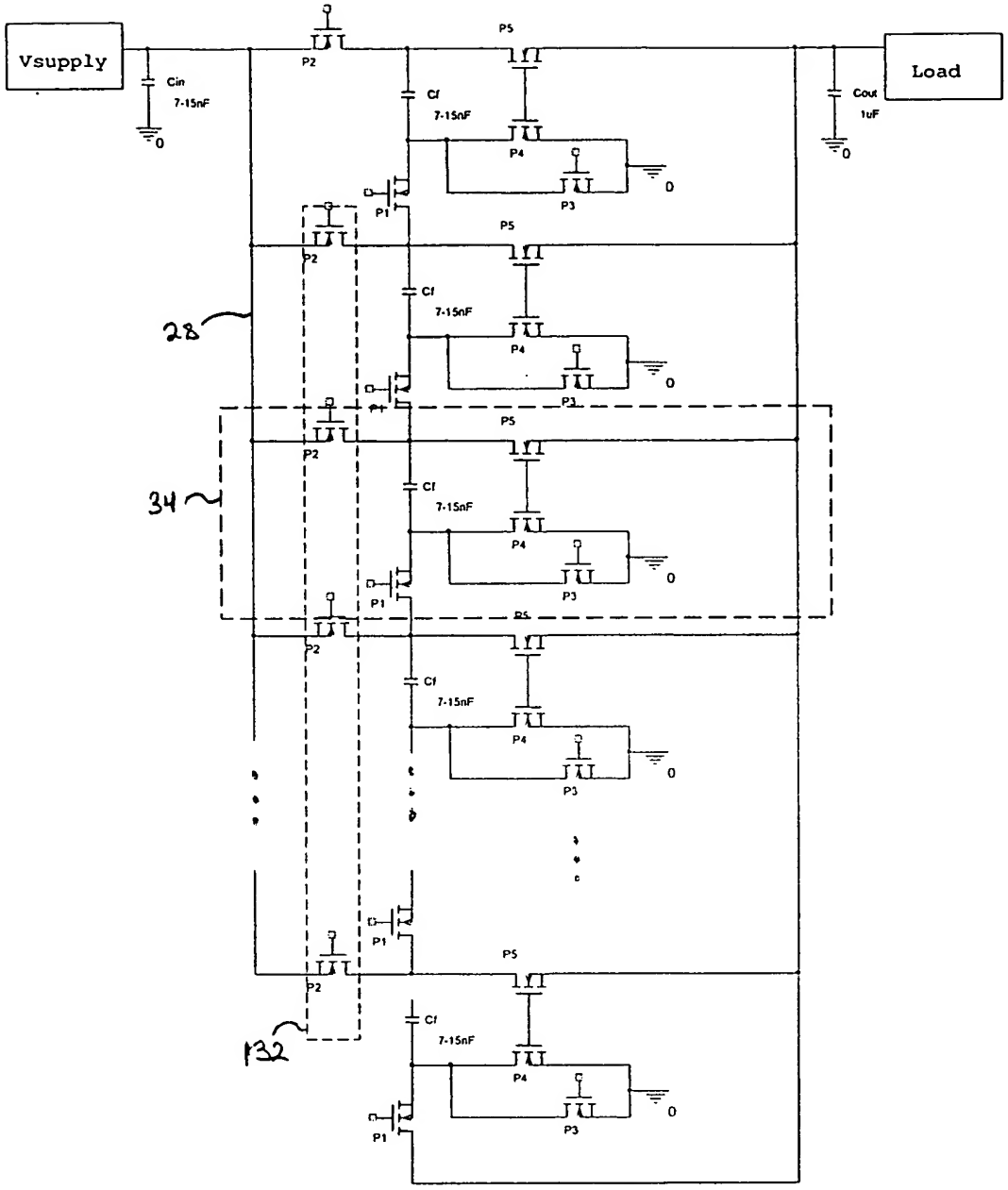
Vsupply
Cin
7-15nF
Load
Cout
1uF
P1
P2
P3
P4
P5
Cf
7-15nF
28
34
132

Fig. 13

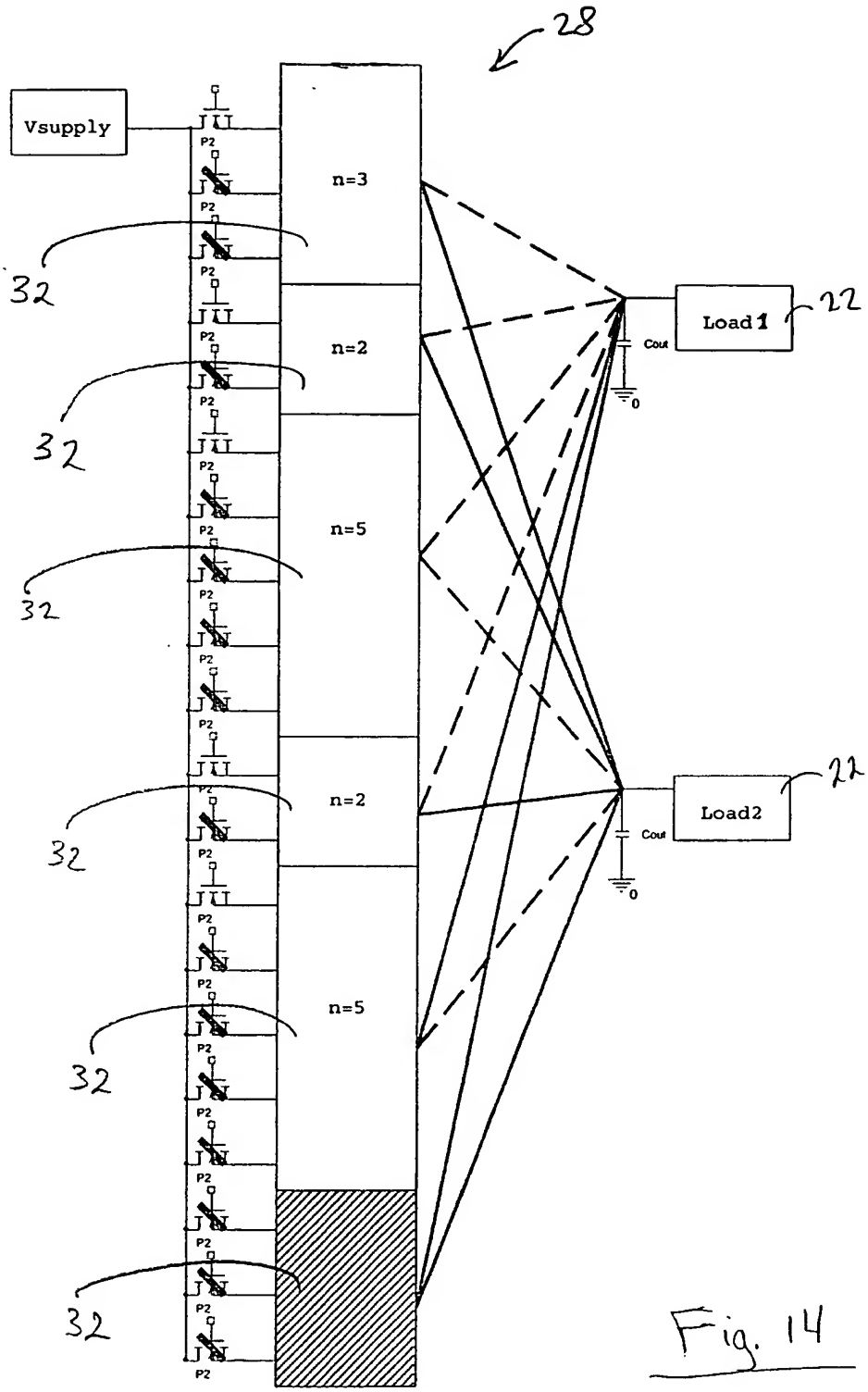

Fig. 14

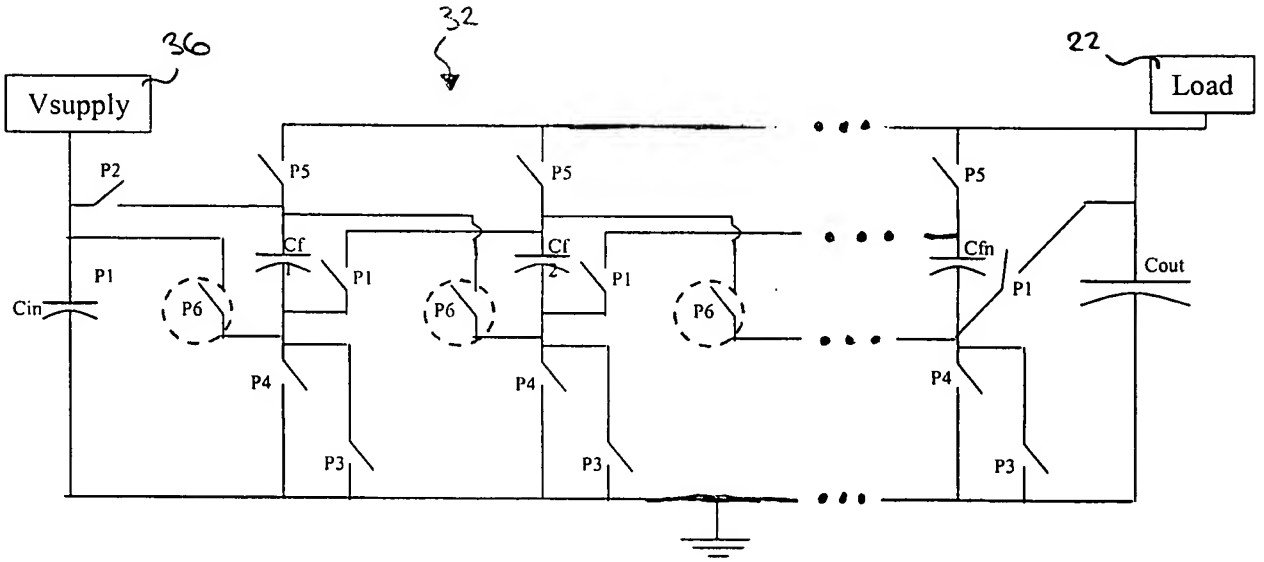
32
36
Vsupply
22
Load
P2
P5
P5
P5
Cf
1
Cf
2
Cfn
Cout
P1
P1
P1
P1
Cin
P6
P6
P6
P4
P4
P4
P3
P3
P3

Fig. 15

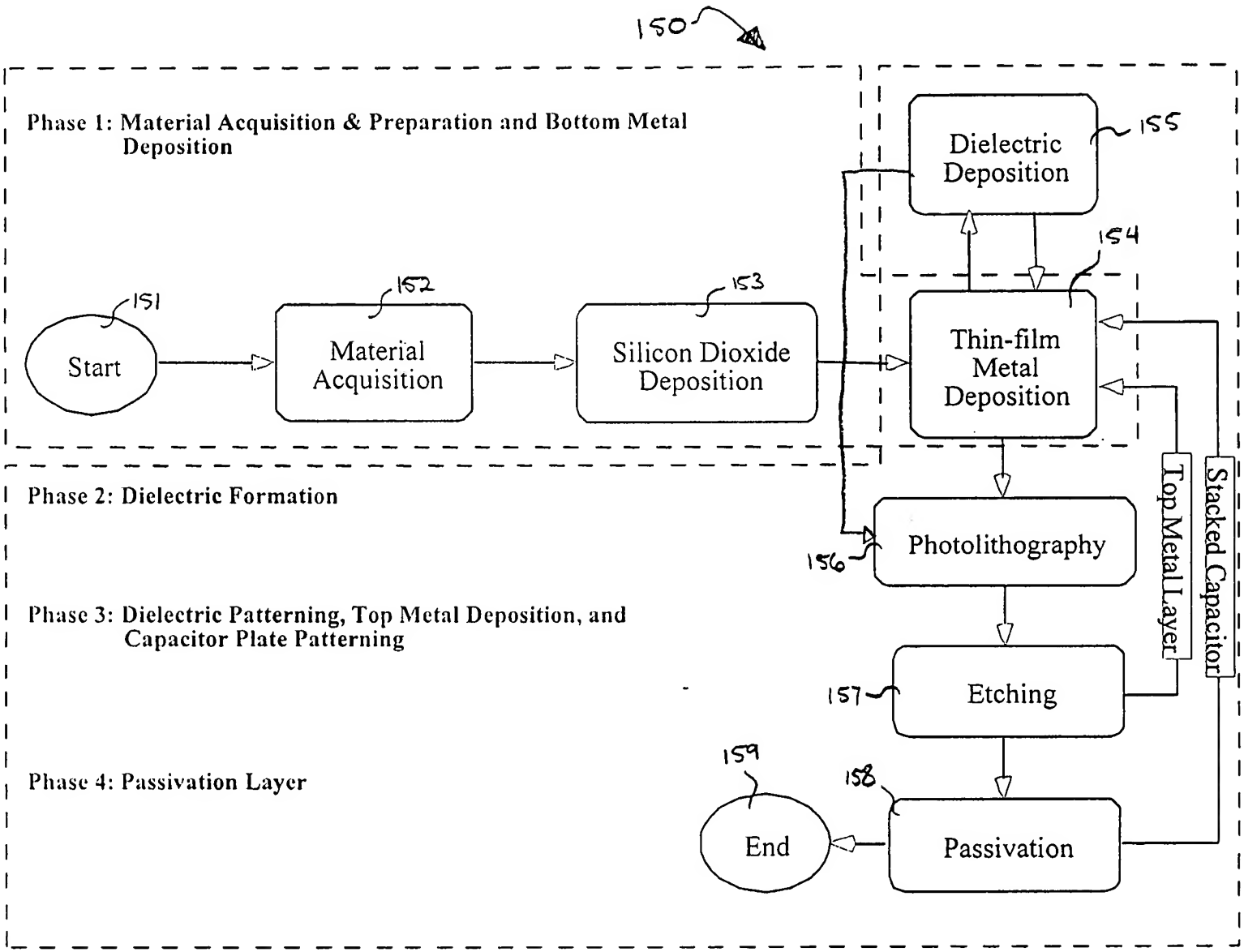
150
Phase 1: Material Acquisition & Preparation and Bottom Metal Deposition
Phase 2: Dielectric Formation
Phase 3: Dielectric Patterning, Top Metal Deposition, and Capacitor Plate Patterning
Phase 4: Passivation Layer
Start
151
Material Acquisition
152
Silicon Dioxide Deposition
153
Thin-film Metal Deposition
154
Dielectric Deposition
155
Photolithography
156
Etching
157
Passivation
158
End
159
Top Metal Layer
Stacked Capacitor

Fig. 16

PHASE	PROCESS STEPS	DESCRIPTION/NOTES	
1	MATERIAL ACQUISITION & PREPARATION		
	Obtain Silicon Wafer	1	Standard 8" Silicon (6"for prototype)
	Deposit SiO2	2	0.5-1.0 µm (insulation and adhesion)
	BOTTOM METAL DEPOSITION		
	Deposit Titanium	1	200 - 500 Å
	Deposit Copper	2	2 microns
	Deposit Tantalum	3	2000 Å
2	DIELECTRIC FORMATION		
	Tantalum Oxide Deposition	1	*Anodization*
3	DIELECTRIC PATTERNING	MASK 1	
	Apply Resist	1	Typically 4 microns
	Exposure	2	Minimum feature size: 20 microns
	Develop	3	
	Etch Tantalum Oxide	4	Typically RIE
	Etch Tantalum	5	Typically RIE
	TOP METAL DEPOSITION		
	Deposit Titanium	1	200 - 500 Å
	Deposit Copper	2	2 microns
	TOP METAL PATTERNING	MASK 2	
	Apply Resist	1	Typically 4 microns
	Exposure	2	Minimum feature size: 20 microns
	Develop	3	
	Etch Copper	4	Wet or dry
	Etch Titanium	5	Wet or dry
	Strip Resist	6	
4	PASSIVATION (OPTIONAL)		
	Apply BCB	1	
	Exposure	2	
	Develop	3	
	Cure	4	

Fig. 17

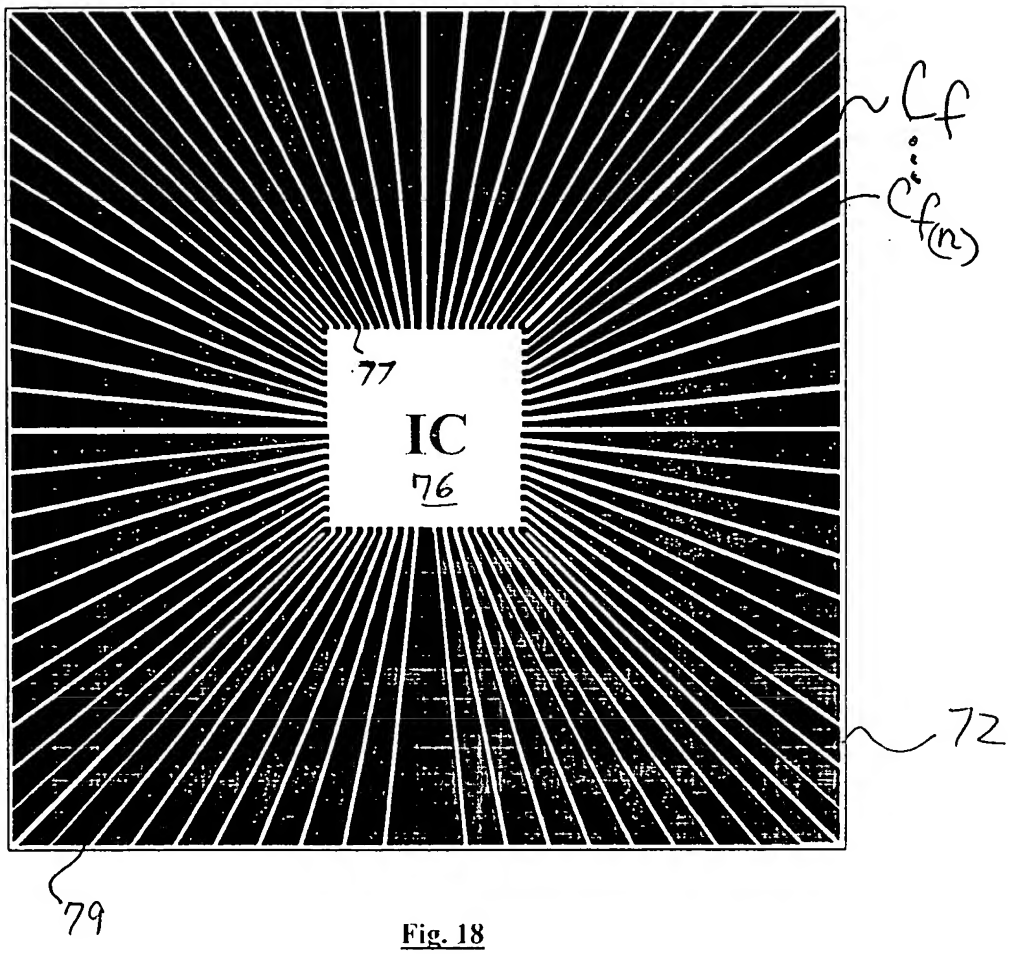

Fig. 18

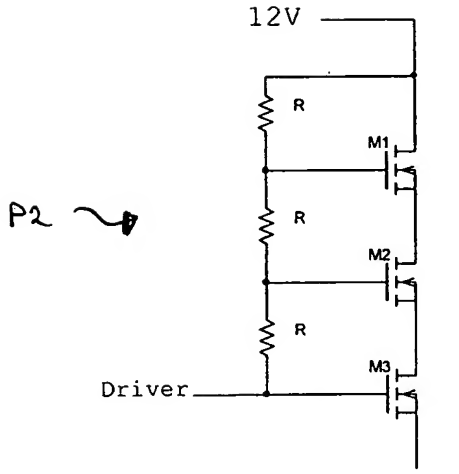

Fig. 19

Input Voltage	Gate Length (Process)	Qg (pC)	Fsw (MHz)
12	0.8 um	>40	1-5
12	0.5 um	27	10-20
5	0.5 um	27	10-20
5	0.35 um	20	20-30
3.3	0.35 um	20	20-30
3.3	0.25 um	10	50-60
3.3	0.18 um	6	80-100

Fig. 20

Transient Up Response

1 A/ns transient. 6 ns [166 MHz] delay to model controller sampling and response

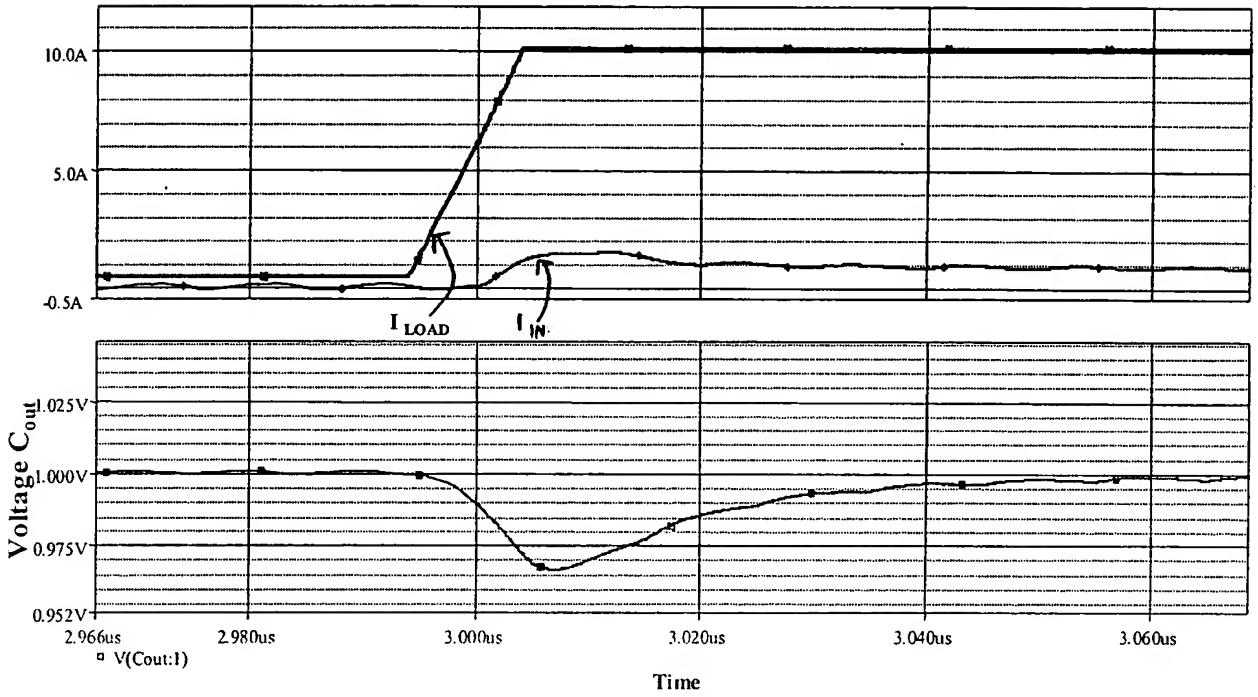

Fig. 21

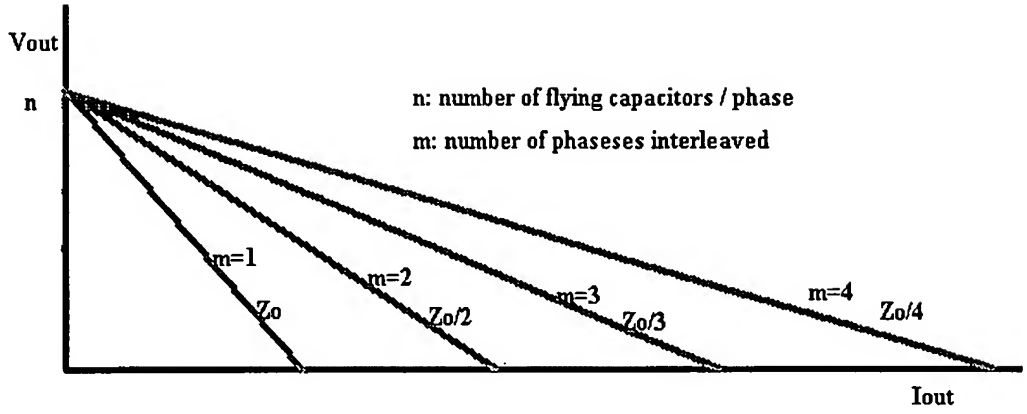
Vout
n
n: number of flying capacitors / phase
m: number of phaseses interleaved
m=1
Zo
m=2
Zo/2
m=3
Zo/3
m=4
Zo/4
Iout

Fig. 22

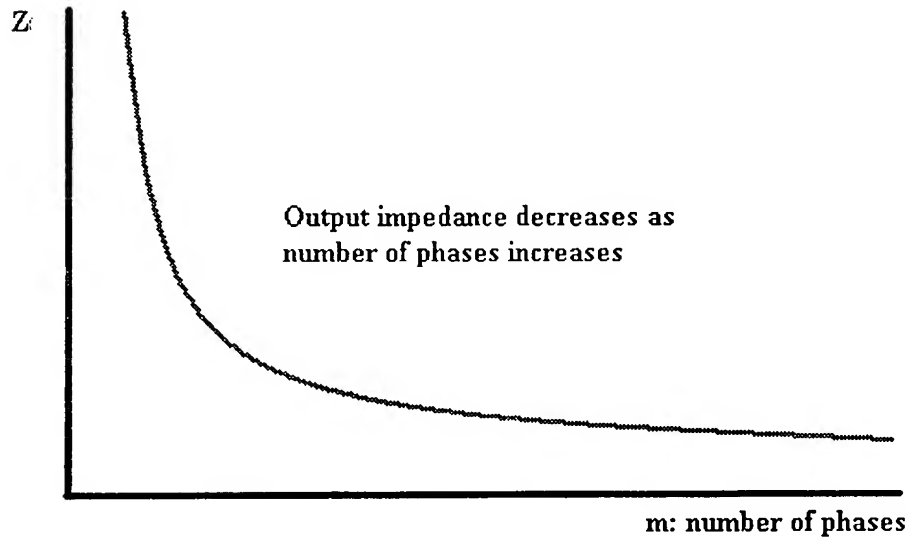
Z
Output impedance decreases as
number of phases increases
m: number of phases

Fig. 23

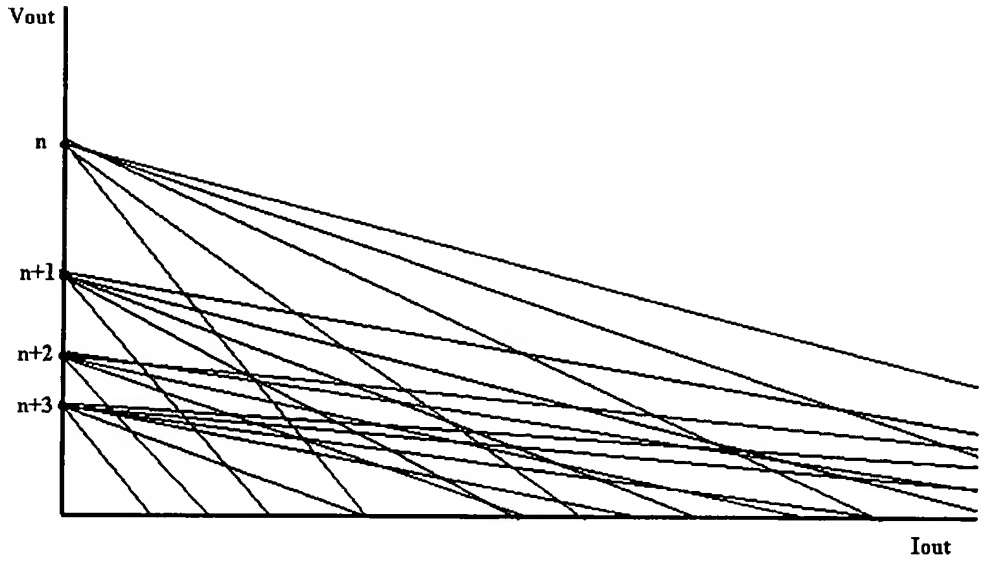
Vout
n
n+1
n+2
n+3
Iout

Fig. 24

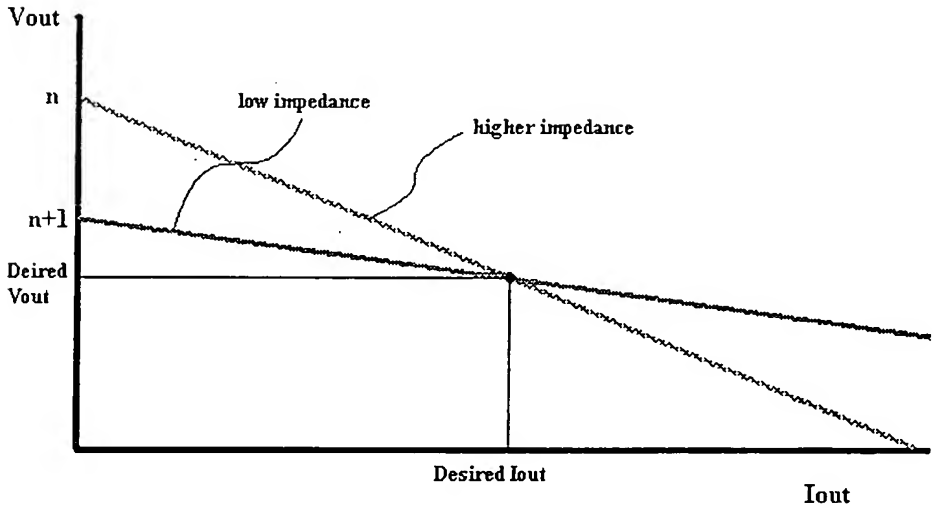
Vout
n
low impedance
higher impedance
n+1
Deired
Vout
Desired Iout
Iout

Fig. 25

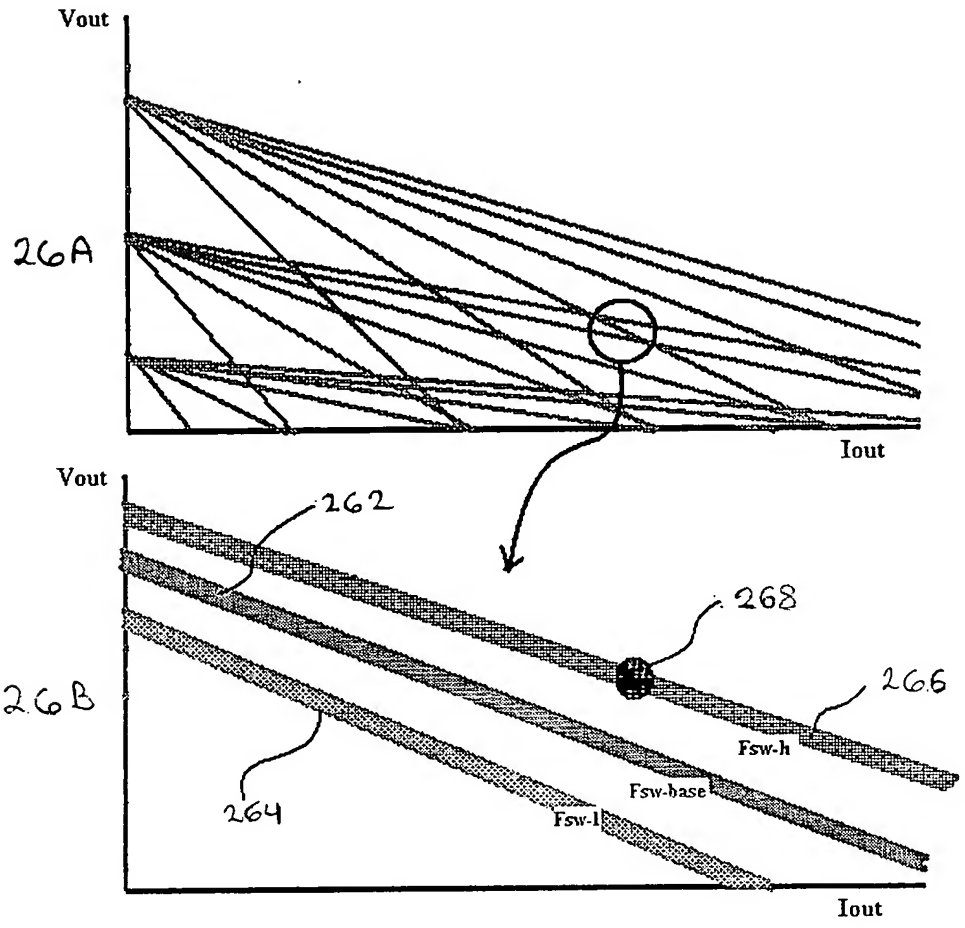

Fig. 26

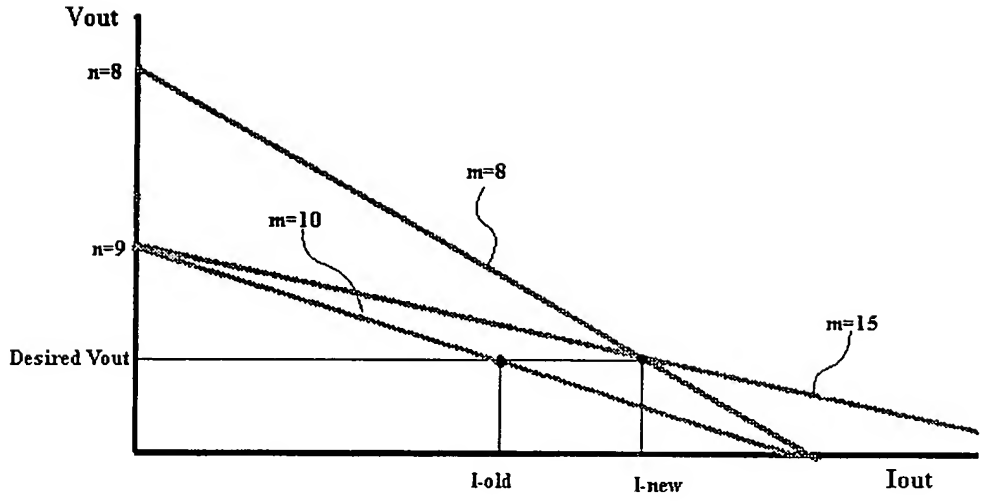

Fig. 27

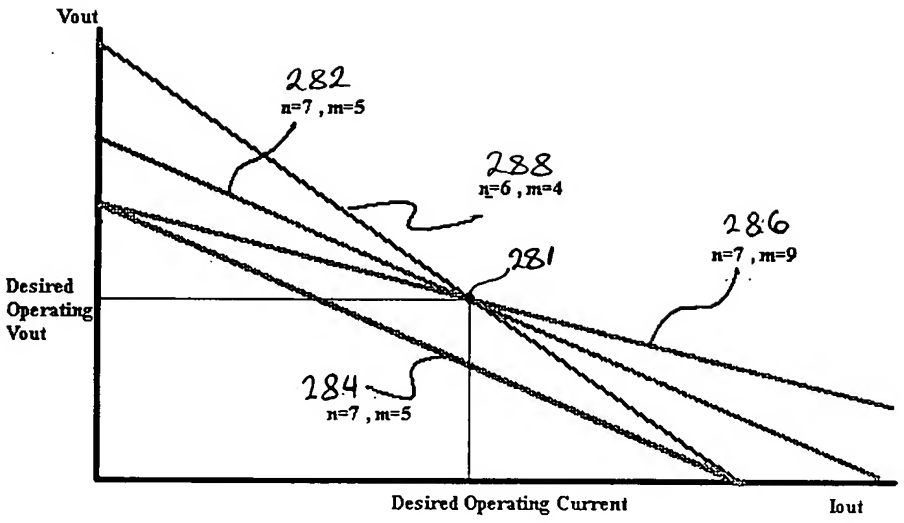
Vout
282
n=7 , m=5
288
n=6 , m=4
286
n=7 , m=9
281
Desired
Operating
Vout
284
n=7 , m=5
Desired Operating Current
Iout

Fig. 28

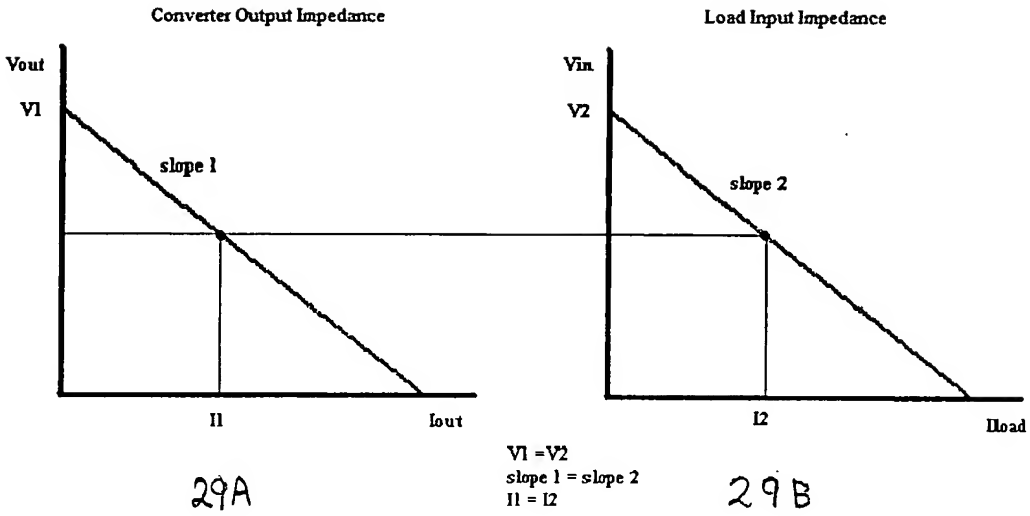
Converter Output Impedance
Load Input Impedance
Vout
V1
slope 1
I1
Iout
29A
Vin
V2
slope 2
I2
Iload
29B
V1 =V2
slope 1 = slope 2
I1 = I2

Fig. 29

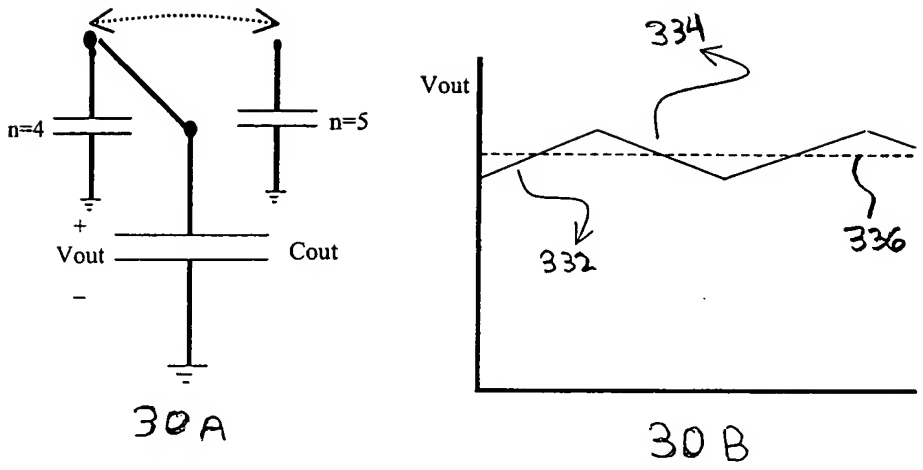

Fig. 30

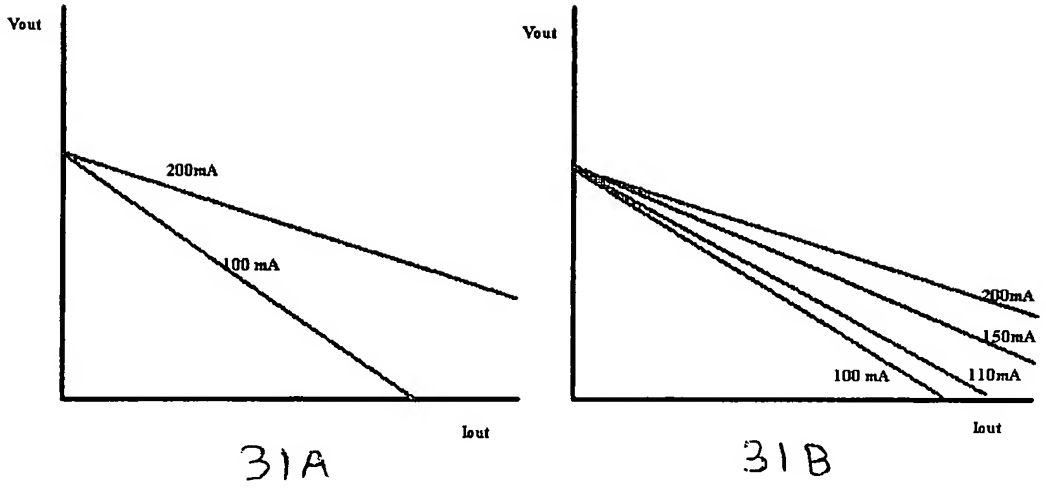
Vout
200mA
100 mA
Iout
31A
Vout
200mA
150mA
100 mA
110mA
Iout
31B

Fig. 31

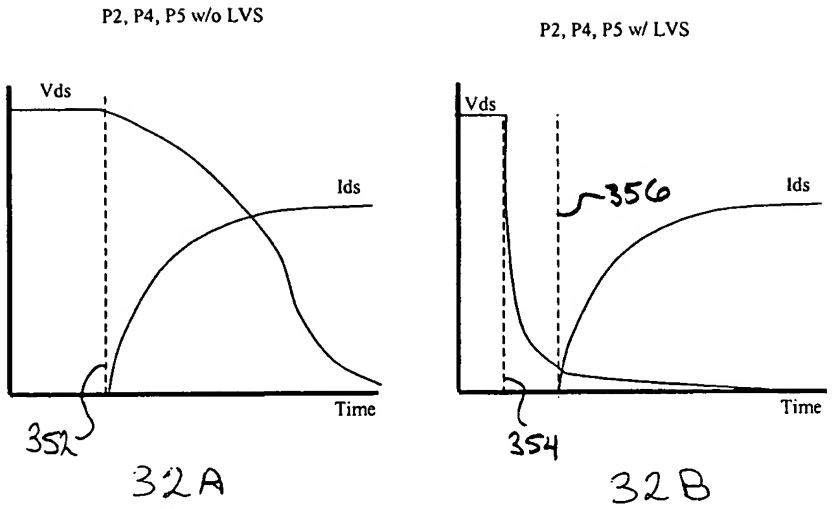
P2, P4, P5 w/o LVS
Vds
Ids
Time
352
32A
P2, P4, P5 w/ LVS
Vds
356
Ids
Time
354
32B

Fig. 32

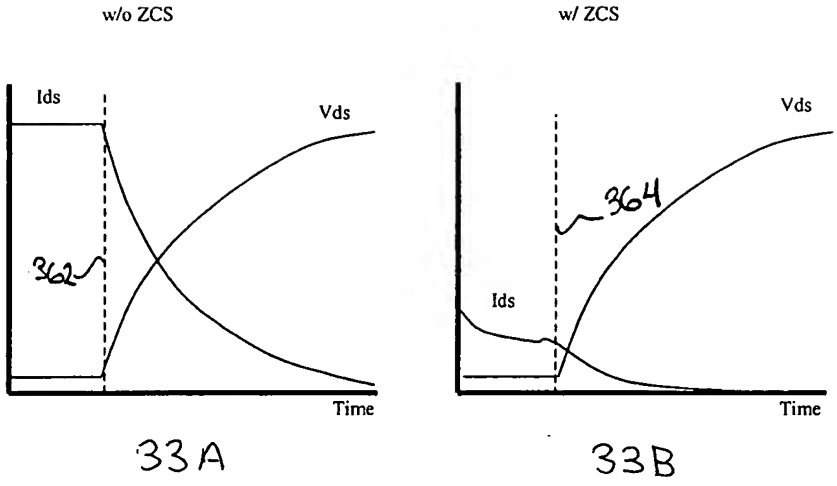

Fig. 33

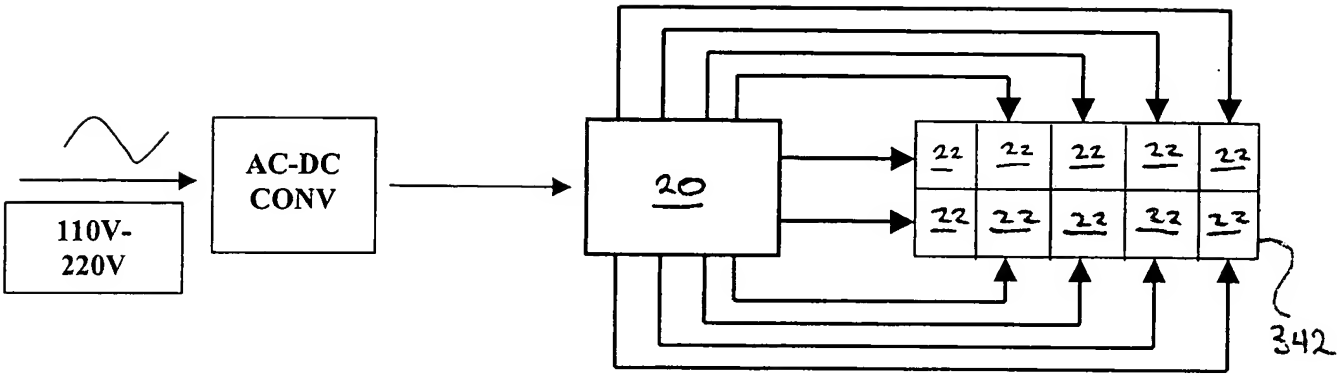

Fig. 34

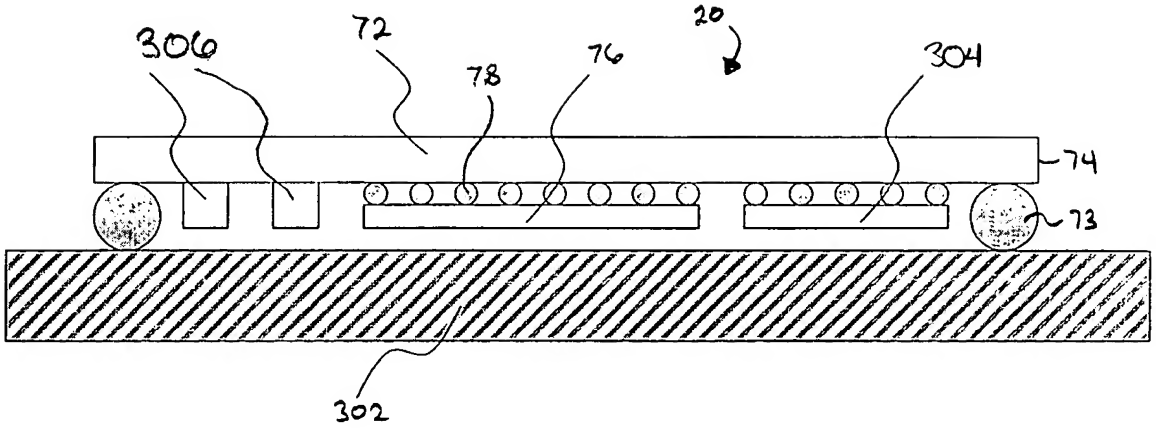

Fig. 35

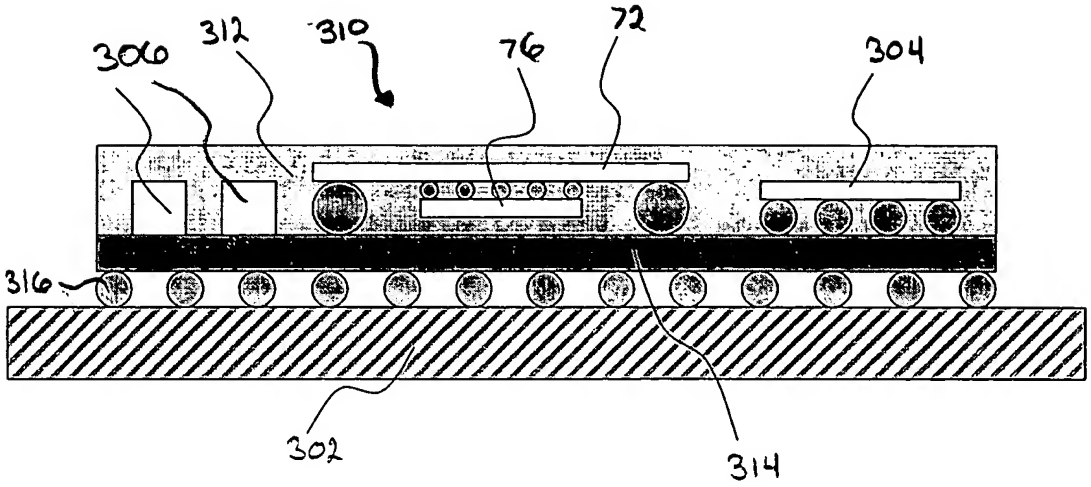

Fig. 36

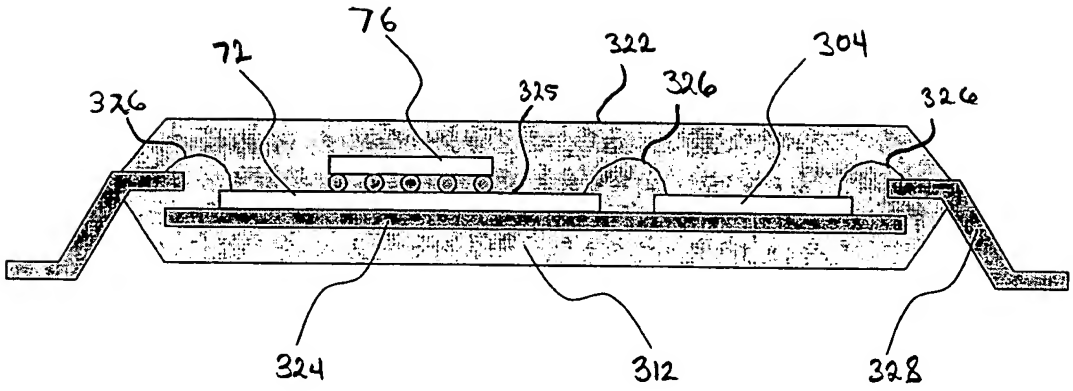

Fig. 37

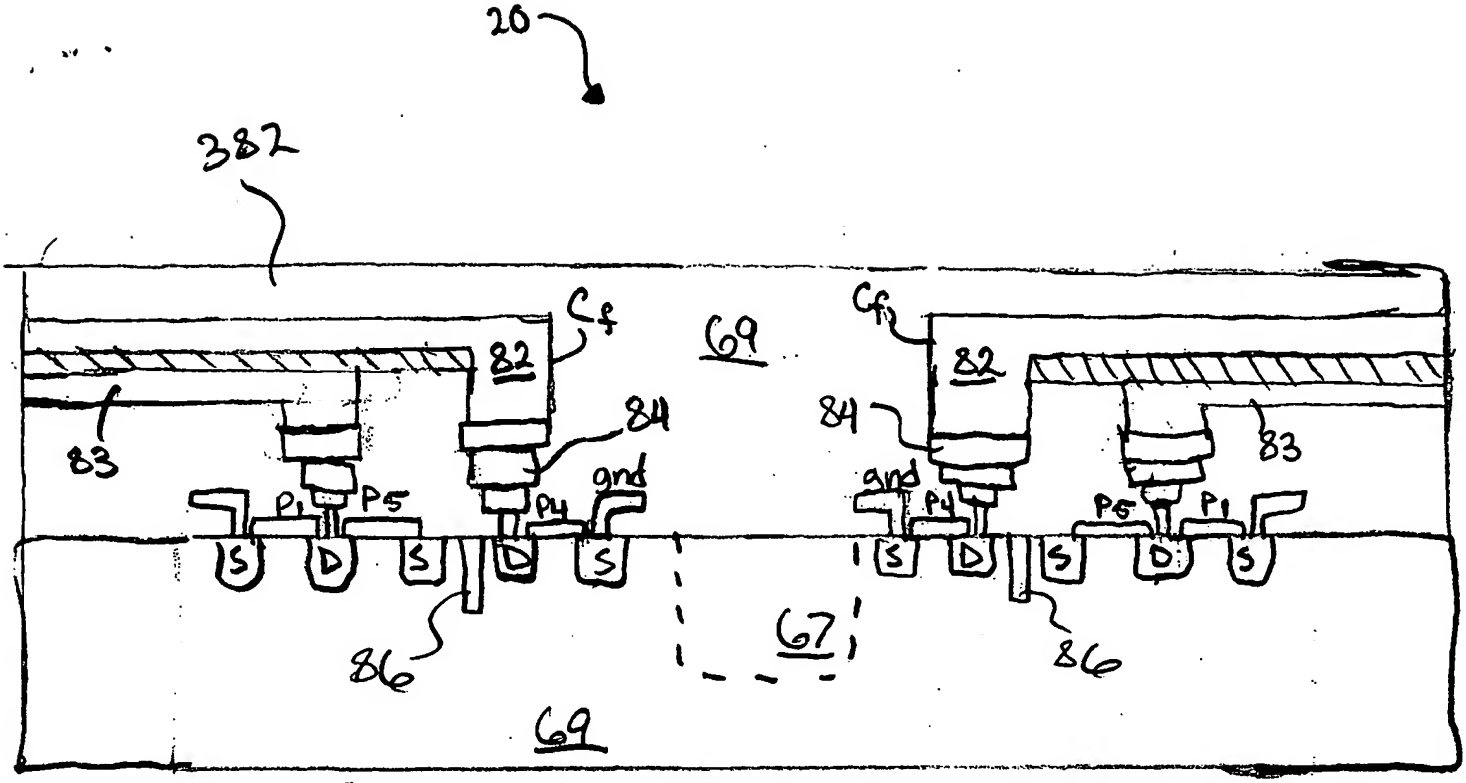

Fig. 38